IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES
(Attorney Docket No. 14532US01)

In the Application of:

Bhatia

Serial No. 10/600,245

Filed: 6/20/2003

For: SYSTEM METHOD AND APPARATUS FOR DECOUPLING VIDEO DECODER AND DISPLAY ENGINE

Examiner: VO

Group Art Unit: 2483

Conf. No.: 5543

Electronically Filed on May 16, 2011

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the final rejection of claims 1-11 and 16-26 of the present application. This Appeal Brief is timely because it is being filed within three months of the February 14, 2011 filing date of the Notice of Appeal and is accompanied by a request for a one-month extension of time.

REAL PARTY IN INTEREST
(37 C.F.R. § 41.37(C)(1)(I))

The real party in interest is Broadcom Corporation, a corporation organized under the laws of the state of California, having a place of business at 5300 California Avenue, Irvine, California 92617, which has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment recorded at Reel 014760, Frame 0347, in the PTO Assignment Search room.

RELATED APPEALS AND INTERFERENCES
(37 C.F.R. § 41.37(C)(1)(II))

Appellant is unaware of any related appeals or interferences.

STATUS OF THE CLAIMS
(37 C.F.R. § 41.37(C)(1)(III))

The present application includes pending claims 1-11 and 16-26 all of which have been rejected. Appellant identifies claims 1-11 and 16-26 as the claims that are being appealed. The text of the pending claims is provided in the Claims Appendix.

STATUS OF AMENDMENTS
(37 C.F.R. § 41.37(C)(1)(IV))

On May 12, 2011, Appellant filed an Amendment Under 37 C.F.R. § 1.116, which included proposed amendments to claims 3, 11 and 26. Specifically, the Amendment proposed changing each occurrence of the term "queue" in claims 3, 11 and 26 to "FIFO." As of the mailing of this Appeal Brief, the Office has not acted on Appellant's May 12 Amendment

SUMMARY OF CLAIMED SUBJECT MATTER
(37 C.F.R. § 41.37(C)(1)(V))

Independent Claim 1 recites the following:

A system[1] for displaying images on a display, said system comprising:

a decoder for decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;[2]

image buffers for storing the decoded images;[3]

a FIFO for storing indicators indicating images to be displayed in a forward display order at normal speed;[4] and

a display engine for presenting the images indicated by the FIFO for display.[5]

Independent Claim 5 recites the following:

A method for displaying images on a display, said method comprising:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;[6]

storing the decoded images;[7]

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[1] *See, e.g.,* Specification at Fig. 1, Ref. 100.
[2] *See, e.g., id.* at p. 7, ¶ 0026, line 1 to p. 8, ¶ 0028, line 11; *see also id.* at Fig. 1, Decoder Engine 115.
[3] *See, e.g., id.* at p. 7. ¶ 0026, lines 8-10; *see also id.* at Fig. 1, Frame Buffers 125a.
[4] *See, e.g., id.* at p. 9, ¶ 0032, lines 1-7; *see also id.* at p. 9, ¶ 0033, lines 12-15; *see also id.* at Fig. 1, FIFO 130; page 9.
[5] *See, e.g., id.* 7, ¶ 0026, lines 1 to p. 8, ¶ 0028, line 11; *see also id.* at Fig. 1, Display Engine 120.
[6] *See, e.g., id.* at p. 9, ¶ 0033, lines 4-6; *see also id.* at Fig. 2, Step 210.

queuing indicators indicating images to be displayed in a FIFO in a forward order of display at normal speed;[8] and

presenting the images indicated by a particular one of the indicators for display.[9]

Independent Claim 8 recites the following:

A circuit[10] for displaying images on a display, said circuit comprising:

a processor;[11]

a memory operably coupled to the processor, said memory storing a plurality of executable instructions, wherein the plurality of executable instructions cause:[12]

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;[13]

storing the decoded images;[14]

storing indicators indicating images to be displayed in a FIFO in a forward order of display at normal speed;[15] and

presenting the images indicated by the stored indicators for display.[16]

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[7] *See, e.g., id.* at p. 9, ¶ 0033, lines 7-9; *see also id.* at Fig. 2, Step 215.
[8] *See, e.g., id.* at p. 9, ¶ 0033, lines 12-15; *see also id.* at Fig. 2, Step 222.
[9] *See, e.g., id.* at p. 9, ¶ 0034, lines 1-9; *see also id.* at Fig. 2, steps 225-235.
[10] *See, e.g., id.* at Figs. 1 and 4.
[11] *See, e.g., id.* at p.13, ¶ 0047, lines 3-5; *see also id.* at Fig. 4, CPU 490.
[12] *See, e.g., id.* at p. 15, lines 1-13.
[13] *See, e.g., id.* at p. 9, ¶ 0033, lines 4-6; *see also id.* at Fig. 2, Step 210.
[14] *See, e.g., id.* at p. 9, ¶ 0033, lines 7-9; *see also id.* at Fig. 2, Step 215.
[15] *See, e.g., id.* at p. 9, ¶ 0033, lines 12-15; *see also id.* at Fig. 2, Step 222.
[16] *See, e.g., id.* at p. 9, ¶ 0034, lines 1-9; *see also id.* at Fig. 2, steps 225-235.

Independent Claim 11 recites the following:

A circuit[17] for displaying images on a display, the circuit comprising:

a first processor;[18]

a first memory operably coupled to the first processor, said first memory storing a plurality of instructions for execution by the first processor, wherein the plurality of executable instructions cause:[19]

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;[20]

storing the decoded;[21]

storing indicators indicating images to be displayed in a FIFO FIFO in a forward order of display at normal speed;[22] and

a second processor operably coupled to the queue;[23]

a second memory operably coupled to the second processor, said second memory storing a plurality of instructions for execution by the second processor, wherein the plurality of executable instructions cause:[24]

presenting the images indicated by the indicators for display.[25]

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[17] *See, e.g., id.* at Figs. 1 and 4.
[18] *See, e.g., id.* at p. 13, line 12; *see also id.* at Fig. 4, MPEG Video Decoder 445.
[19] *See, e.g., id.* at p. 15, lines 1-13.
[20] *See, e.g., id.* at p. 9, ¶ 0033, lines 4-6; *see also id.* at Fig. 2, Step 210.
[21] *See, e.g., id.* at p. 9, ¶ 0033, lines 7-9; *see also id.* at Fig. 2, Step 215.
[22] *See, e.g., id.* at p. 9, ¶ 0033, lines 12-15; *see also id.* at Fig. 2, Step 222.
[23] *See, e.g., id.*, page 13, ¶ 0048, lines 1-9; *see also id.* Fig. 4, Display Engine 450.
[24] *See, e.g., id.* at p. 15, lines 1-13.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(C)(1)(VI))

Claims 1, 5, 8, 11 and 22-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Claims 1-11, 16-21 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. 7,130,526 ("Abelard.") Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abelard in view of U.S. 6,353,700 ("Zhou.")

[25] *See, e.g., id.* at p. 9, ¶ 0034, lines 1-9; *see also id.* at Fig. 2, steps 225-235.

ARGUMENT
(37 C.F.R. § 41.37(C)(1)(VII))

I. THE CLAIMS COMPLY WITH THE STATUTORY REQUIREMENTS OF 35 U.S.C. § 112

A. Claims 1-19 And 22-29 Satisfy The Written Description Requirement

Claims 1, 5, 8, 11 and 22-26 have been rejected under 35 U.S.C. 112, ¶ 1 as purportedly failing to comply with the written description requirement. In this regard, the Examiner states as follows:

> Claims 1, 5, 8, 11, and 22-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. "**a forward order of display at normal speed**" is not disclosed anywhere in the specification; and "**every picture** is displayed" is not disclosed in the specification; "**wherein the queue directly transmits the indicators** from the first processor to the second processor" is not disclosed in the specification

(Final Office Action at 2 (emphasis in original.)) Appellant respectfully traverses this rejection.

1. The Office Has Failed To Establish a Prima Facie Case

As an initial matter, Appellant submits that the Examiner has, by only providing mere conclusory statements, failed to satisfy his burden to articulate a *prima facie* case. Without adequate notice of the basis of this rejection, the burden to rebut this rejection with evidence and/or argument has not yet shifted to Appellant.

The Examiner bears an initial burden of establishing a *prima facie* case when making a written description rejection. *See* MPEP §§ 706.07, 2163 (III)(A). A *prima*

facie case requires a reasonable basis to challenge the adequacy of the written description. *See* MPEP § 2163.04. The MPEP equates this reasonable basis with "a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims." *See* MPEP § 2163(III)(A). Consequently, the Examiner must provide a reasonable basis to reject a claim for failing to satisfy the written description requirement, and this requires "a full development" of the reasons showing that, by a preponderance of the evidence, a person of ordinary skill in the art would not recognize a description of the claimed invention in the disclosure. Mere conclusory statements by the Examiner are insufficient. Rather, every written description rejection "should be stated with a full development of the reasons rather than by a mere conclusion . . . ." *See* MPEP § 706.03. Put another way, the Office must adequately explain the perceived shortcomings of the application so that Appellant is properly notified and able to respond. Finally, until the Office establishes a *prima facie* case, an Appellant is not under an obligation to rebut the rejection. *See* MPEP § 2163.04. Appellant respectfully submits that such is the case here.

In the present instance, the Examiner merely alleges that the claim language in question is not supported by the specification. (Final Office Action at p. 2.) Absent from this rejection, for example, are any "reasoned or supported statements" supporting this rejection, as the MPEP expressly requires. Indeed, the rejection is devoid of "evidence or reasons" as to why the disclosure fails to reasonably convey to one of ordinary skill in the art that Appellant possessed the claimed invention. Thus, the Examiner has failed to set forth express findings of fact that support the lack of written description conclusion

as its own procedures require. *See* MPEP §2163.04. Rather, the provided "reason" is a mere conclusion, which the MPEP expressly warns is insufficient to support this rejection. MPEP § 706.03.

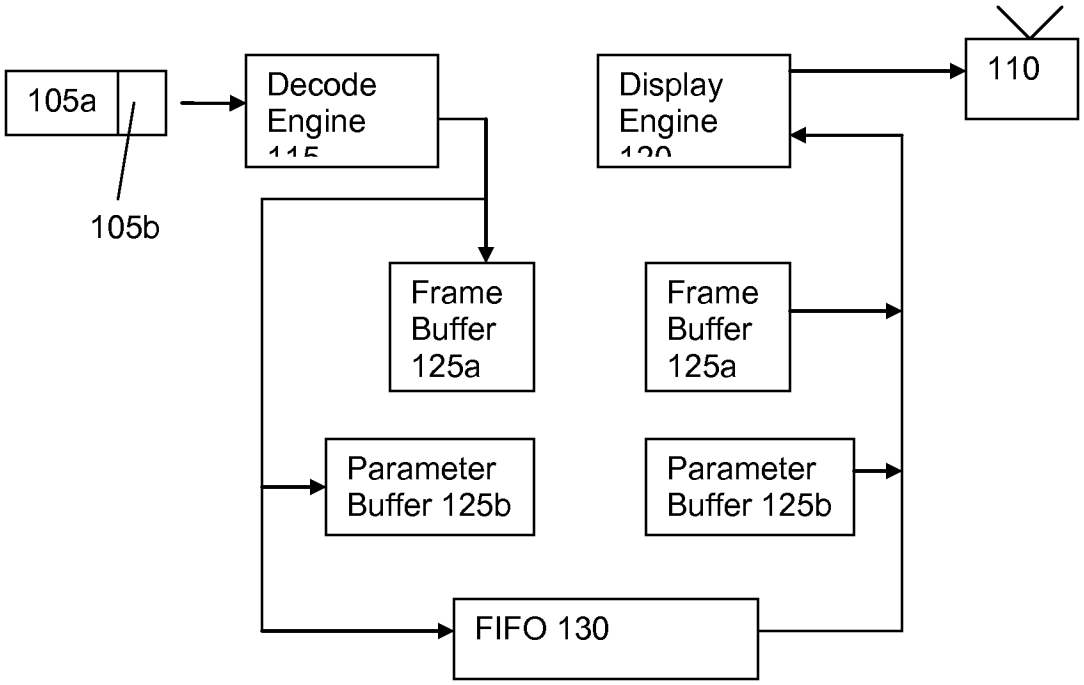
The Examiner's failure to meet his burden to articulate a "reasonable basis challenging the adequacy of the written description" with "findings of fact" is fatal to this rejection since Appellant is under no burden to rebut it. *See* MPEP §§ 706.07, 2163, 2163.04. Accordingly, Appellant respectfully requests that the Board withdraw the rejection of claims 1-19 and 22-29 under the first paragraph of 35 U.S.C. § 112.

2. The Specification Provides Adequate Support For The Claim Terms Identified By The Examiner

Even though the Examiner has failed to establish a *prima facie* case, Appellant will now explain why the terms identified by the Examiner are adequately supported by the specification.

"To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can **reasonably conclude** that the inventor had possession of the claimed invention." MPEP § 2163.[26] This possession may be shown in any number of ways and an Appellant need not describe every claim feature exactly because there is no in *haec verba* requirement. *See* MPEP § 2163. Rather, to satisfy the written description requirement, all that is required is "reasonable clarity." *See* MPEP § 2163.02. Also, an adequate description may be made in any way through express, implicit, or even inherent disclosures in the application, including words, structures, figures, diagrams, and/or formulae. *See* MPEP §§ 2163(I), 2163.02.

Appellant first turns to the phase "wherein the **queue directly transmits the indicators** from the first processor to the second processor" from claim 26. One of ordinary skill in the art would reasonably conclude that Appellant's disclosure adequately described this feature at the time of filing. In this regard, attention is directed to Figure 1 of the application, which is reproduced below:



Specification, FIGURE 1 (Formalized)

As can be seen, the output of Decode Engine 115, e.g., the first processor, feeds directly into FIFO 130. Likewise, the output of FIFO 130 feeds directly into the display engine 120, e.g., the second processor. Accordingly, based on at least this disclosure, Appellant respectfully submits that ordinarily skilled artisans would reasonably conclude that, at the time the application was filed, Appellant possessed the claimed "wherein the

[26] Emphasis added except where noted otherwise.

queue directly transmits the indicators from the first processor to the second processor," as recited in claim 26.

Appellant now turns to the phrase "a forward order of display at normal speed," as recited in claims 1, 5, 8 and 11. This language was added to more clearly distinguish the claims from the "trick mode" described in Abelard. (*See* 9/7/2010 Amendment at 6.) The present application described embodiments of the claimed invention in the context of MPEG and MPEG-2 encoded video. (*See, e.g.,* Application at Figs. 3 and 4; *see also, id.* at ¶¶ 0035-0043.) A person of ordinary skill in the art would appreciate that the default (or standard) mode for displaying MPEG and MPEG-2 encoded video is at normal speed in the forward direction. For example, when playing a recorded television show from a DVR, the default is to play the video in the forward direction at normal speed. Other display functions, such as pause, fast forward, fast rewind, slow forward, slow rewind, jump to previous/future frame etc., are referred to in the art as trick modes. Trick mode functions typically require additionally storage and processing steps in comparison to displaying the video in normal mode. Accordingly, Appellant respectfully submits that ordinarily skilled artisans would reasonably conclude that, at the time the application was filed, Appellant possessed the claimed "storing [or queuing0 indicators indicating images to be displayed in a **forward display order at normal speed**," as recited in claim 1, 5, 8 and 11.

Appellant turns next to the phrase "**every picture** is displayed," as recited in claims 22-25. As in the preceding paragraph, Appellant submits a person of ordinary skill in the art would appreciate that the norm in the context of MPEG and MPEG-2 encoded video is to display every picture. Accordingly, Appellant respectfully submits

that ordinarily skilled artisans would reasonably conclude that, at the time the application was filed, Appellant possessed the claimed limitation that "every picture is displayed," as recited in claims 22-25.

In view of the above, Appellant submits claims 1-19 and 22-29 satisfy the written description requirement. Accordingly, Appellant respectfully requests that the Board withdraw the rejection of claims 1-19 and 22-29 under the first paragraph of 35 U.S.C. § 112, ¶ 1.

II. CLAIMS 1-11, 16-21 AND 26 ARE PATENTABLE OVER ABELARD

A. Independent Claims 1, 5, 8, 11

Claim 1 is patentable over Abelard at least because Abelard fails to disclose "a decoder for decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images," as required by claim 1. In rejecting claim 1, the Examiner states as follows regarding this limitation:

> Re claims 1 and 5, Abelard discloses . . . a decoder (9 of fig. 1, a video decoder, col. 4, lines 14-20) for decoding encoded images and parameters associated with the images (DECODING MANAGER of fig. 1, there are parameters for decoding as shown in figure 5, I, B, P parameters), thereby resulting in decoded images and decoded parameters associated with the decoded images (26 of fig. 1, A, B, and C are decoded memories to store the decoded image and the decoded parameters, fig. 7, A memory stored 12, P8, B"1, B"0, P5, B9, P5, I'2, P'2, P'8, Bl, BO accordance to decoding per frame period) . . . .

(Final Office Action at 3.) The passage of Abelard cited by the Examiner reads as follows:

> Compressed data destined to the video decoder 9 is stored in an input bit buffer 25, from where it is read as appropriate by the decoder 9. Reconstructed pictures are stored in a reconstruction memory 26, which is accessed by the decoder for both reading and writing. The reconstruction memory according to the invention has three buffers (A, B, C), each corresponding to one decoded picture.

(Abelard at 4:14-20.) Nothing in this passage discloses or suggests that the decoder 9 decodes parameters associated with decoded images. In this regard, the Examiner contends, "[element] 26 of fig. 1, A, B, and C are decoded memories to store the decoded image and the decoded parameters." However, the cited passage of Abelard merely indicates that "each buffer correspond[s] to one decoded picture." Hence, at most Abelard indicates the buffers stores images. Abelard does not, however, disclose that the buffers also store parameters associated with the images.

In the above passage, the Examiner also apparently contends that Figure 7 illustates decoded parameters, as recited in claim 1. Even if this were true, which Appellant does not concede, there is no suggestion that the decoder 9 decodes these "parameters." Nor, does the Examiner identify any text from Abelard to support this contention.

Moreover, elsewhere Abelard states as follows:

> Each single picture that must be decoded (whether subsequently to be displayed or not) must be transmitted to the video decoder 9. All the necessary information to access the compressed content is supplied in the trickmode information tables. The Stream Access Manager is in charge of transferring the picture data identified by the Overall Trickmode Control from memory 5, to the video decoder, transferring only relevant information among that read from the hard disk drive by the Streaming Driver. For each picture to be decoded, the Stream Access Manager will be notified by the Overall Trickmode Control.

(Abelard at 5:9-10.) Hence, Abelard teaches that information for accessing the images is supplied to the decoder 9. Abelard does not disclose or suggest that the decoder 9 subsequently decodes this information.

Accordingly, claim 1 is patentable at least because Abelard fails to disclose "**a decoder for decoding** encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images," as required by claim 1.

In addition, claim 1 is patentable because Abelard fails to disclose or suggest "a FIFO for storing indicators indicating images to be displayed in a forward display order at normal speed . . . ," as recited in claim 1. In rejecting claim 1, the Examiner contends as follows:

> Re claims 1 and 5, Abelard discloses . . . a FIFO (DISPLAY MANAGER of fig. 2, col. 5, lines 37-42; col. 5, lines 43-col. 6, line 10; fig. 3) for storing indicators (the descriptors are shared by the decoding manager and the display manager, col. 5, lines 43-46) indicating images to be displayed (col. 6, lines 39-51, identifying the next picture to be displayed; col. 6, lines 66-col. 7, line 3) in a forward display order at normal speed (col. 6, lines 66-col. 7, line 3; note In forward mode, Next(N) returns the ID of following picture to be displayed according to normal display order (i.e. in respect to the temporal reference). In backward mode. Next(N) returns the ID of the previous picture according to normal display order) . . . .

(Final Office Action at 4.) In the above passage, the Examiner apparently equates the "descriptors" discussed in column 5 to the "indicators" recited in claim 1. Abelard these software descriptors as:

> A software descriptor of each reconstruction buffer reflects the state of each buffer. These descriptors are shared by the Video Decoding Manager and the Display Manager. Before programming a decoding, the Video Decoding manager tests

> if the reconstruction buffer that must receive this picture is available. If it is not, then the Video Decoding Manager waits for the Display Manager to release the buffer. Then, the decoding in this buffer can be programmed and the buffer access can be locked again.

(Abelard at 5:43-51.) Hence, Abelard merely discloses "descriptors" that reflect the state of the buffers (A, B, C). Abelard does not, however, disclose that the "descriptors are indicators . . . indicating the next image to be displayed," as the Examiner alleges.

The Examiner also cites to Abelard's Next(N) function, which is described in the patent as follows:

> The trickmode information according to the present embodiment is a data structure comprising linked items. It is made of Picture descriptors linked with each other according to their order in the stream. The reader is reminded that the stream as received (and in this case as recorded) contains pictures in decoding order, not display order. Each Picture descriptor gives details about a picture in the MPEG coded stream as well as enough information to locate the compressed material of the picture on the storage unit. Each picture in the stream is identified with a particular Picture ID. In FIGS. 3 and 4, "N" is such a picture ID and a function `Next(N)` returns a picture ID. The Next(N) function's processing is based on an analysis of the trickmode Information, given the type of trickmode to be displayed.
>
> In forward mode, Next(N) returns the ID of following picture to be displayed according to normal display order (i.e. in respect to the temporal reference). In backward mode. Next(N) returns the ID of the previous picture according to normal display order.
>
> For fast operation (forward or backward), pictures must be skipped, so Next(N) returns IDs of non-consecutive pictures.
>
> The Next(N) function is implemented by the Overall Trickmode Control module which, knowing N, uses the trickmode tables defined in the already mentioned patent application to access all data required to decode a picture.

(Abelard at 6:52-7:10.) In the above passage, Abelard discusses picture descriptors, which "[give] details about a picture in the MPEG coded stream as well as enough information to locate the compressed material of the picture on the storage unit." These picture descriptors are not the same as the software descriptors discussed in column 5 of Abelard. (*See* Abelard at 5:43-51.) Nor is there any indication that the Picture descriptors are ever stored in a FIFO for indicating images to be displayed in a forward display order at normal speed. The above passage of Abelard also discusses picture IDs that are used identify particular pictures. It is unclear, whether the picture IDs and picture descriptors are one in the same or different elements. Regardless, there is no disclosure or suggestion that the picture IDs are stored in a FIFO for indicating images to be displayed in a forward display order at normal speed. Rather, the above passage explains how the Next(N) command processes trickmode information to return an appropriate picture ID.

Accordingly, claim 1 is also patentable because Abelard fails to disclose or suggest "a FIFO for storing indicators indicating images to be displayed in a forward display order at normal speed . . . ," as recited in claim 1.

Independent claims 5, 8 and 11 are similar in relevant respect to claim 1. Therefore, claims 5, 8 and 11 are patentable for at least the reasons stated above regarding claim 1.

In addition, claim 11 requires "a first processor . . . [and] a second processor operably coupled to the [FIFO] . . . ." In rejecting claim 11, the Examiner alleges the claimed first and second processors are met by Abelard's microprocessor 10 and video processing circuitry 14. However, there simply in no indication that element 14 of

Abelard is a separate processor. Nor has the Examiner identified any disclosure from Abelard to support this construction. Accordingly, claim 11 is also patentable for at least this additional reason.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claims 1, 5, 8 and 11.

B. Claims 2, 6, 9

Claims 2, 6 and 9 depend on independent claims 1, 5 and 8, respectively. Therefore, claims 2, 6 and 9 are patentable over Abelard for at least the reasons stated above with regard to claims 1, 5 and 8.

Claim 2 also requires "parameter buffers for storing the decoded parameters associated with the images." Since, as discussed above in connection with claim 1, Abelard does not disclose decoding parameters associated with the images, Abelard necessarily cannot disclose "storing the decoded parameters," as required by claim 2.

Claims 6 and 9 are similar in relevant respect to claim 2. Therefore, claims 6 and 9 are patentable for at least the reasons stated above regarding claim 2.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claims 2, 6 and 9.

C. Claims 3, 7 and 10

Claims 3, 7 and 10 depend on independent claims 1, 5 and 8, respectively. Therefore, claims 3, 7 and 10 are allowable over Abelard for at least the reasons stated above with regard to claims 1, 5 and 8.

In addition, claim 3 requires "receiving the decoded parameters and displaying the decoded images based on the decoded parameters." Since, as discussed above, Abelard fails to disclose or suggest decoding parameters associated with the images, Abelard necessarily cannot disclose "receiving the decoded parameters and displaying the decoded images based on the decoded parameters," as required by claim 3.

Claims 7 and 10 are similar in relevant respect to claim 23. Therefore, claims 7 and 10 are patentable for at least the reasons stated above regarding claim 3.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claims 3, 7 and 10.

D. Claim 4

Claim 4 depends on independent claim 1. Therefore, claim 4 is patentable over Abelard for at least the reasons stated above with regard to claim 1.

In addition, claim 4 requires "wherein the decoder comprises a first processor and the display engine comprises a second processor." In rejecting claim 4, the Examiner states as follows:

> Abelard further discloses wherein the decoder comprises a first processor (9 of fig. 1) and the display engine comprises a second processor (14 of fig. 1).

(Final Office Action at p. 4.) Initially, Appellant notes that the Examiner's rejection of claim 4 is inconsistent with the position taken in rejecting claim 11. Specifically, in rejecting claim 11, the Examiner identifies Abelard's microprocessor 10 as the first processor, while in claim 10 the Examiner identifies the decoder 9 as the first processor. In any event, although the decoder 14 and video processing circuitry 14 are illustrated

as separate boxes in Abelard's Figure 1, there simply is no suggestion that the decoder 9 and video processing circuitry 14 are embodied in separate processors. Nor has the Examiner cited to any disclosure from Abelard to support this contention. Accordingly, claim 4 is also patentable for this additional reason.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claim 4.

E. Claims 17-20

Claims 17-20 depend on independent claims 1, 5, 8 and 11, respectively. Therefore, claims 17-20 are allowable over Abelard for at least the reasons stated above with regard to claims 1, 5, 8 and 11.

In addition, claim 17 requires that "each indicator [stored in the FIFO] indicates a different image to be displayed." Since, Abelard does not disclose storing indicators in a FIFO (as required by claim 1), Abelard necessarily cannot disclose "each indicator [that is stored in the FIFO] indicates a different image to be displayed," as required by claim 2.

Claims 18-20 are similar in relevant respect to claim 17. Therefore, these claims are patentable for at least the reasons stated above regarding claim 17.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claims 17-20.

F. Claim 21

Claim 21 ultimately depends on independent claim 11. Therefore, claim 21 is patentable over Abelard for at least the reasons stated above with regard to claim 11.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claim 21.

G. Claim 26

Claim 26 ultimately depends on independent claim 1. Therefore, claim 26 is patentable over Abelard for at least the reasons stated above with regard to claim 1.

In addition, claim 26 requires that "the queue directly transmits the indicators from the first processor to the second processor." In rejecting claim 4, the Examiner cites to column 5, lines 43-46. In context, this passage reads as follows:

> A software descriptor of each reconstruction buffer reflects the state of each buffer. These descriptors are shared by the Video Decoding Manager and the Display Manager. Before programming a decoding, the Video Decoding manager tests if the reconstruction buffer that must receive this picture is available. If it is not, then the Video Decoding Manager waits for the Display Manager to release the buffer. Then, the decoding in this buffer can be programmed and the buffer access can be locked again.

(Abelard at 5:43-51.) As discussed above in connection with claim 1, the software descriptors discussed in this passage of Abelard are not equivalent to the claimed indicators, nor are they stored in a FIFO. Further, although the above passage states that "[t]hese descriptors are shared by the Video Decoding Manager and the Display Manager," there simply is no disclosure, in the cited passage or elsewhere, that the software descriptors are directly transmitted from the first processor to the second

processor via a FIFO. Accordingly, claim 26 is also patentable for this additional reason.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claim 26.

III. CLAIMS 22-25 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF ABELARD AND ZHOU

A. Claims 22-25

Claims 22-25 depend on independent claims 1, 5, 8 and 11, respectively. Therefore, claims 22-25 are allowable over Abelard for at least the reasons stated above with regard to claims 1, 5, 8 and 11. Zhou fails to overcome the deficiencies noted above with regard to Abelard. Accordingly, claims 22-25 are patentable over Abelard and Zhou for at least the reasons stated above in connection with claims 1, 5, 8 and 11

In addition, claim 22 requires that "each indicator [stored in the FIFO] indicates a different image to be displayed." The Examiner admits that Abelard fails to explicitly disclose this limitation. The Examiner turns to Zhou in an attempt to make up for this admitted deficiency of Zhou. However, in proposing to combine Abelard and Zhou, the Examiner fails to provide "articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness" in the detailed manner described in KSR.

Specifically, in order to support an assertion of obviousness, the Examiner is required to provide "some articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness." *See KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) quoting *In re Kahn*, 441 F.2d 997,988 (CA Fed.

2006). Put another way, the Examiner should "identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, 127 S. Ct. at 1741. The Examiner should make "explicit" this rationale of "the apparent reason to combine the known elements in the fashion claimed," including a detailed explanation of "the effects of demands known to the design community or present in the marketplace" and "the background knowledge possessed by a person having ordinary skill in the art." *Id.*

In the present instance, the Examiner attempts to justify the combination of Abelard and Zhou as follows:

> Re claims 22-25, Abelard teaches the display for display video pictures based on the identification, but not every picture is displayed.
>
> However, Zhou teaches every frame is displayed after only one MPEG decoding process (col. 6, lines 39-50).
>
> Therefore, taking the teachings of Abelard and Zhou together as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Zhou into Abelard to improve display order.

(Final Office Action at p. 8.) This conclusory sentence is the entire extent of the Examiner's justification for alleging that it would be obvious to combine Abelard and Zhou. This conclusory allegation does not provide "articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness" in the detailed manner described in *KSR*. In this regard, the Examiner provides absolutely no explanation of how Zhou would "improve display order" in the system of Abelard. Instead, the Examiner appears to propose this combination based solely on improper hindsight. Hence, it is respectfully submitted that the Examiner has not established a

prima facie case of obviousness and the Board should withdraw the rejection of claim 22.

Claims 23-25 are similar in relevant respect to claim 22. Therefore, these claims are patentable for at least the reasons stated above regarding claim 22.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claims 22-25.

CONCLUSION

Appellant respectfully submits that the pending claims of the present application should be in condition for allowance for at least the reasons discussed above, and requests reconsideration of the claim rejections. The Commissioner is authorized to charge the any necessary or credit overpayment to Deposit Account 13-0017.

Respectfully submitted,

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/Kirk A. Vander Leest/
Kirk A. Vander Leest
Registration No. 34,036

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100

CLAIMS APPENDIX
(37 C.F.R. § 41.37(c)(1)(viii))

1. A system for displaying images on a display, said system comprising:

a decoder for decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;

image buffers for storing the decoded images;

a FIFO for storing indicators indicating images to be displayed in a forward display order at normal speed; and

a display engine for presenting the images indicated by the FIFO for display.

2. The system of claim 1, further comprising:

parameter buffers for storing the decoded parameters associated with the images.

3. The system of claim 2, wherein the display engine presents the images indicated by the queue for display by receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

4. The system of claim 1, wherein the decoder comprises a first processor and the display engine comprises a second processor.

5. A method for displaying images on a display, said method comprising:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;

storing the decoded images;

queuing indicators indicating images to be displayed in a FIFO in a forward order of display at normal speed; and

presenting the images indicated by a particular one of the indicators for display.

6. The method of claim 5, further comprising:

storing the decoded parameters associated with the images.

7. The method of claim 6, wherein presenting the images for display further comprises receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

8. A circuit for displaying images on a display, said circuit comprising:

a processor;

a memory operably coupled to the processor, said memory storing a plurality of executable instructions, wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;

storing the decoded images;

storing indicators indicating images to be displayed in a FIFO in a forward order of display at normal speed; and

presenting the images indicated by the stored indicators for display.

9. The circuit of claim 8, further comprising:

storing the decoded parameters associated with the images.

10. The circuit of claim 9, wherein the instructions causing presenting the images further comprise instructions causing receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

11. A circuit for displaying images on a display, said circuit comprising:

a first processor;

a first memory operably coupled to the first processor, said first memory storing a plurality of instructions for execution by the first processor, wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;

storing the decoded images;

storing indicators indicating images to be displayed in a FIFO, in a forward order of display at normal speed; and

a second processor operably coupled to the queue;

a second memory operably coupled to the second processor, said second memory storing a plurality of instructions for execution by the second processor, wherein the plurality of executable instructions cause:

presenting the images indicated by the indicators for display.

12-15. (Cancelled)

16. The system of claim 1, wherein the FIFO stores the indicators in a particular order, and wherein the display engine displays the images associated with the indicators in an order corresponding to the order that the indicators are stored in the FIFO.

17. The system of claim 1, wherein each indicator indicates a different image to be displayed.

18. The method of claim 5, wherein each indicator indicates a different image to be displayed.

19. The circuit of claim 8, wherein each indicator indicates a different image to be displayed.

20. The circuit of claim 11, wherein each indicator indicates a different image to be displayed.

21. The circuit of claim 16, wherein the FIFO stores the indicators in the particular order prior to the display engine displaying the images associated with the indicators in the order corresponding to the order that the indicators are stored in the FIFO.

22. The system of claim 1, wherein every picture is displayed.

23. The method of claim 5, wherein every picture is displayed.

24. The circuit of claim 8, wherein every picture is displayed.

25. The circuit of claim 11, wherein every picture is displayed.

26. The system of claim 4, wherein the queue directly transmits the indicators from the first processor to the second processor.

EVIDENCE APPENDIX
(37 C.F.R. § 41.37(c)(1)(ix))

- U.S. Patent No. 7,130,526 ("Abelard") entered into the record in the Office Action mailed June 4, 2010.

- U.S. Patent No. 6,353,700 ("Zhou") entered into the record in the Office Action mailed October 13, 2010.

RELATED PROCEEDINGS APPENDIX
(37 C.F.R. § 41.37(c)(1)(x))

Appellant is unaware of any related appeals or interferences.